WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Thursday, July 08, 2004

Hide?	Set Name	Query	Hit Count
		DB=USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR	
☐	L28	l13 and L22	8
☐	L27	l11.clm. and L22	2
☐	L26	l11 and L22	23
☐	L25	l3.ab. and L22	3
☐	L24	l3 and L22	28
☐	L23	l8 and L22	5
☐	L22	l16 or l17 or l18 or l19 or l20 or l21	2532
☐	L21	713/600.ccls.	579
☐	L20	713/503.ccls.	328
☐	L19	713/502.ccls.	574
☐	L18	713/501.ccls.	580
☐	L17	713/500.ccls.	542
☐	L16	713/400.ccls.	716
☐	L15	L13 and ((multipl$9 near3 clock$4) same (distribut$9 near3 clock$4))	3
☐	L14	L13 and (multipl$9 near3 clock$4)	15
☐	L13	L11 and (distribut$9 near3 clock$4)	31
☐	L12	L11 same (distribut$9 near3 clock$4)	0
☐	L11	l1 with ((plurality or multiple) near2 (processors or units or devices))	469
☐	L10	l1 same ((plurality or multiple) near2 (processors or units or devices))	699
☐	L9	l1 same (field adj bus)	4
☐	L8	l1 and (field adj bus)	52
☐	L7	l3 and (field adj bus)	0
☐	L6	l3 same (field adj bus)	0
☐	L5	L1 same (multipl$9 near3 (system adj clock$4))	7
☐	L4	L1 same (distribut$9 near3 (system adj clock$4))	3
☐	L3	L1 same (system adj clock$4)	356
☐	L2	L1 same (system clock$4)	10726
☐	L1	(synchroniz$9 near3 (process$4 or task$4))	22252

END OF SEARCH HISTORY

L27: Entry 1 of 2 File: USPT Nov 3, 1998

DOCUMENT-IDENTIFIER: US 5832253 A
TITLE: Multiprocessors system for selectively wire-oring a combination of signal lines and thereafter using one line to control the running or stalling of a selected processor

Current US Cross Reference Classification (3):
713/400

CLAIMS:

1. A computer system having a plurality of processor units, each processor unit connected to other processor units for parallel and independent processing, each processor unit processing instructions having no required relationship to instructions processed in other processor units, each of said processor units connected in common to a plurality of signal lines and directly responsive to instructions so as to be capable of setting a first signal level on a combination of said lines, monitoring at least one of said combination of said lines for a second signal level, and stalling or continuing processing in response to said second signal level on said one of said combination of said lines so that said processor units are selectively synchronized with other processor units through said one of said combination of said lines.

17. In a computer system having a plurality of processor units, each processor unit connected for parallel and independent processing of instructions having no required relationship to instructions processed in other processor units, each processor unit connected in common to a plurality of signal lines and capable of setting a first signal level on each of said lines and monitoring said each of said lines in response to instructions to said processor, a method of synchronizing operations between said processor units comprising:

directly instructing each processor unit processing a set of related operations to set one of said lines, including instructing at least one processor unit processing a plurality of related operation sets to set a plurality of said lines;

directly instructing each processor unit processing a set of related operations to release a line upon completion of its set of related operations; and

directly instructing at least one of said processor units to monitor said line to determine completion of said set of related operations, and to stall or to continue processing responsive to a second level on said line so that said processor units handling said set of related operations are selectively synchronized at the completion of said set of related operations.

L27: Entry 2 of 2 File: USPT May 22, 1990

DOCUMENT-IDENTIFIER: US 4928234 A
TITLE: Data processor system and method

Current US Cross Reference Classification (3):
713/400

CLAIMS:

1. A data processing system of the type having a system bus, including a bus clock, one or more data input means for inputting data, display means for displaying inputted data and processed data, storage means for storing the input data and the processed data, and shared storage means connected to each of the above means through the system bus, the system processing data as designated by the data input means, wherein the system comprises

(a) a plurailty of memory bank means, each of which is connected to the system bus and which together constitute the shared storage means;

(b) a plurality of separate processor means provided for each of the data input means, the display means and the data storage means, respectively, for separately processing data for each of them, each of the separate processor means being connected to the system bus and being capable of generating a memory request command signal on the system bus for the purpose of transferring data between itself and any one of the memory bank means;

(c) arbitration means within the shared storage means which is responsive to a memory request command signal generated by one of the processor means for generating separate enable signals to acknowledge occupation of one of the memory bank means by the one processor means which generated the memory request; and

(d) data dividing means for dividing data transferred between the one processor means and the one memory bank means into predetermined groupings of divisional data and for processing each divisional data in synchronization with the bus clock of the system bus and in simultaneous parallel fashion when a plurality of memory requests are out-putted simultaneously from a plurality of the processor means.

2. A data processing system of the type having a system bus, including a bus clock, one or more data input means for inputting data, display means for displaying inputted data and processed data, storage means for storing the input data and the processed data, and shared storage means connected to each of the above means through the system bus, the system processing data as designated by the data input means, wherein the system comprises

(a) a plurality of memory bank means, each of which is connected to the system bus and which together constitute the shared storage means;

(b) a plurality of separate processor means provided for each of the data input means, the display means and the data storage means, respectively, for separately

processing data for each of them, each of the separate processor means being connected to the system bus and being capable of generating a memory request command signal on the system bus for the purpose of transferring data between itself and any one of the memory bank means;

(c) arbitration means within the shared storage means which is responsive to a memory request command signal generated by one of the processor means for generating separate enable signals to acknowledge occupation of one of the memory bank means by the one processor means which generated the memory request, the arbitration means including means for generating a sequence of separate timing signals whose periods define "time slots" and allocating the time slots to the plurality of memory bank means in sequence and synchronously with the bus clock of the system bus so that for each memory bank means there is a corresponding time slot, and wherein the enable signals are generated during the corresponding time slots; and

(d) data dividing means for dividing data transferred between the one processor means and the one memory bank means into predetermined groupings of divisional data and for processing each divisional data in synchronization with the bus clock of the system bus and in simultaneous parallel fashion when a plurality of memory requests are out-putted simultaneously from a plurality of the processor means and wherein the data dividing means transfers divisional data between the one processor means and the one memory bank means through the system bus during a predetermined number of time slots after the time slot allocated to the one memory bank means.

12. A method of processing data using a data processing system of the type having a bus clock, a system bus and an address bus, the method being of the type having the steps of inputting data, storing data, processing data, and displaying data wherein the improvement comprises the steps of:

(a) storing data in a plurality of memory banks which are connected to each other by the system bus;

(b) separately processing data for each of the steps of inputting, storing, and displaying data, in separate data processors, each of the separate processing steps being carried out over the system bus, and outputting a memory request command signal on the system bus from one of the data processors for the purpose of transferring data between one of the memory banks and the one data processor;

(c) occupying the one memory bank while transferring data between the one processor and the one memory bank and generating an enable signal to acknowledge the occupation; and

(d) simultaneously outputting a plurality of memory requests from a plurality of processors, dividing data to be transferred between the processors and the memory banks into predetermined groupings of divisional data, and processing each divisional data in synchronization with the bus clock of the system bus and in simultaneous parallel fashion.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L25: Entry 1 of 3 File: USPT Dec 4, 2001

DOCUMENT-IDENTIFIER: US 6327667 B1
TITLE: Apparatus and method for operating clock sensitive devices in multiple timing domains

Abstract Text (1):
In a digital signal processing system, such as a computer system, an apparatus for communicating digital signals in a plurality of operating domains. The first domain has first timing and control signals synchronized to a first clock. In response to an event, the apparatus dynamically transitions the operation of the synchronous memory to a second domain having second timing and control signals synchronized to a second clock. The first timing and control signals being different in frequency, shape, and protocol than the second timing and control signals. The first clock can be a processor clock to synchronize communication of address and data signals with a processor, and the second clock can be a system clock to synchronize communication of address and data signals with an asynchronous data processing device such as random access memory.

Current US Original Classification (1):
713/500

Current US Cross Reference Classification (1):
713/600

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L25: Entry 2 of 3 File: USPT Aug 1, 2000

DOCUMENT-IDENTIFIER: US 6098178 A
TITLE: Time synchronization algorithm for massively parallel processor systems

Abstract Text (1):
A time synchronized multi-processor system and a method for determining the absolute time when an event occurs in the system are described. The sys has a plurality of processor elements, a system clock for generating a periodic time signal which is received by each of the processor elements, event reports generated by at least one of the processor elements, a system controller for reading the event reports, and a time board for generating an interrupt signal which causes the system controller to read the event report and to determine the absolute time of the event. The method for determining the absolute time when the event occurs in the system comprises the steps of providing a plurality of processor elements, providing a system clock for generating a time signal, detecting an event and providing at least one processor element with a signal representative of the event, generating an event report with the processor(s) and periodically generating a second or interrupt signal using a time board for causing a system controller board to search for any such event report, read the event report, and determine the absolute time of day of any event in the event report.

Current US Original Classification (1):
713/500

Current US Cross Reference Classification (1):
713/502

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

End of Result Set

Generate Collection Print

L25: Entry 3 of 3 File: USPT Aug 9, 1988

DOCUMENT-IDENTIFIER: US 4763297 A
TITLE: Monolithic integrated digital circuit including an internal clock generator and circuitry for processing multi-digit signals

Abstract Text (1):
A monolithic integrated digital circuit including at least one circuit for the serial data processing of multi-digit data signals synchronized to a clock system, the serial data processing circuits using a clock signal coming from a clock oscillator which is also integrated. The clock oscillator includes an odd number of ring-connected inverting stages. The output of the oscillator is provided to a counter. When the counter counts a number of pulses equal to the number of digits of the output signal of the data processing circuit, the counter stops the clock oscillator. The system clock signal is applied to both the reset input of the counter and the synchronizing input of the data processing circuit.

Current US Original Classification (1):
713/400

Current US Cross Reference Classification (1):
713/501

Previous Doc Next Doc Go to Doc#

L15: Entry 2 of 3 File: USPT Sep 17, 1996

DOCUMENT-IDENTIFIER: US 5557224 A
**** See image for Certificate of Correction ****
TITLE: Apparatus and method for generating a phase-controlled clock signal

Brief Summary Text (9):
Furthermore, microprocessors typically include some logic, such as a bus interface unit, that operates at the external system clock frequency. Therefore, there is a great need for an improved clock regenerator that generates and distributes both the previously mentioned high-speed internal processor clock signal and an internal system clock signal throughout the microprocessor. Both of these clocks should be distributed throughout the microprocessor using the same distribution network. Therefore, the improved clock generator should be capable of generating and distributing multiple in-phase clock signals within the microprocessor.

Brief Summary Text (10):
Finally, even if an improved clock regenerator could be implemented, either one of two substantially equal, but 180 degrees out of phase, processor clock signals will be generated each time a reset or power-up event occurs. This event produces testing errors and degrades performance of systems having multiple processors that must operate in synchronization with each other. Accordingly, there is a great need for an improved clock regenerator that generates an internal processor clock signal that is consistently synchronized with the external system clock signal.

Detailed Description Text (3):
System bus 11 includes data lines, a system clock line, and a hard reset ("Hreset") line (not shown). The Hreset line and the system clock lines are connected to clock generator 200 of the present invention, while the data lines are connected to bus interface unit ("BIU") 12. The Hreset line goes HIGH and then LOW to initiate a system reset or power-on condition. BIU 12 controls the transfer of information between processor unit 20 and system bus 11. Clock generator 200 generates and distributes an internal processor clock signal to, for example, processor unit 20. Similarly, clock generator 200 generates and distributes an internal system clock signal to, for example, BIU 12. These clock signals are generated in response to the system clock line of system bus 11.

Detailed Description Text (22):
AND gate 277 "ANDs" sel.sub.-- neg 284 and inverted Hreset.sub.-- 1 240. In turn, OR gate 278 "ORs" the output of AND gate 277 and freeze.sub.-- qsm signal 286. AND gate 279 "ANDs" the output of OR gate 278 and an inverted Hreset 215 which, in turn, is latched by master slave latch 282. CR 281 regenerates and distributes clock signal 232 to master/slave latch 282. As such, during negative cycles of that clock, the master latch opens and the slave latch latches the output of AND gate 279 to generate selecting signal sel.sub.-- neg 284. Conversely, during positive cycles of that clock, the slave latch opens and the master latch latches the output of AND gate 279, which is inverted by invertor 283 to generate selecting signal sel.sub.-- pos 285.

CLAIMS:

14. The method according to claim 13 further comprising the step of distributing

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
End of Result Set

Generate Collection Print

L15: Entry 3 of 3 File: USPT May 26, 1992

DOCUMENT-IDENTIFIER: US 5117442 A
TITLE: Methods and circuits for synchronizing signals in a modular redundant fault tolerant computer system

Brief Summary Text (8):
In addition to clock skew, the TMR system must be able to cope with early or late arrival or non-arrival of one or more signal input events. It is known in the art that if a transition event is presented to the inputs of two or more clocked circuits (e.g., edge-latched D-type flip-flops), the corresponding event appearing at their outputs may differ in time (signal timing divergence). If the signal timing divergence becomes as great as one clock period, cycle skipping can occur. This is especially likely if the input changes near the minimum setup time to a clock edge, and the clock signals are skewed by a finite amount or the logic delays of the flip-flops differ slightly. Thus, even a single event can cause discrepancies when multiple clocks, or distributed versions of a single clock, are used in a TMR or Pair system. There is an even greater likelihood of discrepancy when multiple events or multiple copies of a single event must be coordinated, as in a TMR or Pair system. Another problem which can occur is metastability of a flip-flop, where its output becomes indeterminate when its input changes near the minimum setup time to a clock edge, for example. It is also known that if a component, wire or solder connection fails, an expected event may not arrive when and where expected.

Brief Summary Text (14):
U.S. Pat. No. 4,330,826 to Whiteside et al. discloses a synchronizer module for each processor of a fault-tolerant multiple computer system in which a sampling period is timed, the majority vote of the samples from the processors is taken, and the sampling period is adjusted so that its end will approximately coincide with the end of the sampling periods of the other processors. While the synchronizer modules permit late starting of one or more processors in the system, and is intended to identify processors which are out of synchronization with the system for fault-detection purposes, it does not appear to synchronize the logical signals of multiple processors within the bounds of the skew between clock signals of the processors.

Brief Summary Text (15):
Further, U.S. Pat. No. 4,589,066 to Lam et al. discloses fault-tolerant synchronization for multiple processor systems in which majority voting is used to determine whether synchronizing pulses arrive within a predetermined time window defined by a counter, indicating synchronization between multiple processors. Since the synchronization is linked to a time window, it has the disadvantage of being less fine-grained than may be desired.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L4: Entry 2 of 3 File: USPT Jul 14, 1998

DOCUMENT-IDENTIFIER: US 5781558 A
TITLE: Diagnostic memory access

Abstract Text (1):
A data processing system has at least one processing module containing one or more blocks of memory, having control registers which are accessible via a diagnostic interface, and a clock module which distributes system clocks to the processing module(s), the operation of which is controllable using a similar diagnostic interface. One of the possible actions in the clock module is the generation of a single-shot clock pulse. A diagnostic control unit is connected to the separate diagnostic interfaces of the processing module(s) and the clock module, and is capable of simultaneously controlling the two diagnostic interfaces in such a way that a single-shot clock pulse can be synchronized with the diagnostic access to a processing module to effect the loading or dumping of a block of memory line by line.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

End of Result Set

Generate Collection Print

L4: Entry 3 of 3 File: USPT May 31, 1988

DOCUMENT-IDENTIFIER: US 4748644 A
TITLE: Method and apparatus for a constant frequency clock source in phase with a variable frequency system clock

Abstract Text (1):
A clock apparatus provides variable frequency system clock signals for synchronizing the operation of data processing apparatus and constant frequency timing signals, in phase with the system clock signals, for controlling the operation of an interval timer or related apparatus. The variable frequency system clock signals are produced by placing a controllable divider network in the phase locked loop. The input signals to the controllable divider network are distributed as the system clock signals. The constant frequency is obtained by distributing count signals from the controllable divider network of the phase locked loop circuit to a plurality of comparator circuits and output signals from the comparator provide a multiplicity of timing intervals that result in the constant frequency signals. The timing intervals are determined by the control signals that are applied to controllable divider network and to a plurality of divider circuits associated with the comparator circuits. The control signal is divided by the divider circuit and the resulting value entered in the comparator circuit where the value is compared with the count from the controllable divider network. A distribution network, used to provide a delay in the distribution of the system clock signals, thereby synchronizing components of the data processing system, is placed in the phase locked loop to insure that the signal to the constant frequency signals and the system clock signals are in phase.

Previous Doc Next Doc Go to Doc#

L5: Entry 1 of 7 File: USPT Mar 30, 2004

DOCUMENT-IDENTIFIER: US 6715096 B2
TITLE: Interface circuit device for performing data sampling at optimum strobe timing by using stored data window information to determine the strobe timing

Detailed Description Text (157):
FIG. 52 schematically shows a whole structure of a data processing system according to a fourth embodiment of the invention. In this data processing system shown in FIG. 52, memory control unit 2 is integrated with a logic (or processor) 104 on the same chip. A processing device 100 also includes a PLL (Phase-Locked Loop Circuit) 102, which receives clock signal (system clock) CLK from clock generator 3, and produces an internal operation clock signal PCLK through frequency multiplication of system clock CLK. Internal operation clock signal PCLK generated from PLL 102 has a frequency of, e.g., 1 GHz, and determines the operation speed of logic 104. In other words, internal operation clock signal PCLK determines a processing cycle of logic 104, and logic 104 executes the processing in synchronization with this operation clock signal PCLK. Operation clock signal PCLK for logic, produced by PLL 102, is also supplied to a strobe timing adjusting circuit 110. Strobe timing adjusting circuit 110 receives data Dc read from memory devices 1a-1n, and detects the effective data period in accordance with operation clock signal PCLK for logic. Similarly to the first embodiment, strobe timing adjusting circuit 110 determines a strobe timing in accordance with the detected effective data period, and produces a strobe signal for taking data into input circuit 7.

L5: Entry 3 of 7 File: USPT Mar 26, 2002

DOCUMENT-IDENTIFIER: US 6363490 B1
TITLE: Method and apparatus for monitoring the temperature of a processor

Detailed Description Text (16):
External clock 102 of FIG. 1 provides a clock signal to processor 100. The clock signal is used to synchronize the processing and communication of information by processor 100. Clock 102 may be the clock source such as the system clock, or a clock multiplier or other type of clock buffer that receives, processes, and re-transmits a clock signal.

L5: Entry 5 of 7 File: USPT Feb 9, 1999

DOCUMENT-IDENTIFIER: US 5870595 A
TITLE: Clock-supply control system of digital-signal processors

Brief Summary Text (5):
FIG. 10 is a block diagram showing the configuration of a conventional digital-signal processing block. Reference numeral 1 shown in the figure is the digital-signal processing block and reference numeral 2 is a data input unit for inputting data 3. Reference numeral 4 is a digital-signal processor, referred to hereafter simply as a DSP, for inputting data 5 from the data input unit 2 and carrying out digital processing on the data 5 in synchronization with a clock signal 6. Reference numeral 7 is a data output unit for inputting data 8 from the DSP 4 and outputting data 9 to a circuit at the next stage. Reference numeral 10 is a frequency multiplier for multiplying the frequency of a system clock signal 11 in order to generate the clock signal 6 for driving the operation of the DSP 4.

Brief Summary Text (8):
FIG. 10 is a diagram showing a digital-signal processing block having an embedded DSP 4 for carrying out such processing. Data 3 supplied to the data input unit 2 is transferred to the DSP 4 as data 5 with appropriate timing. The DSP 4 carries out digital processing on the data 5 in synchronization with the clock signal 6 in accordance with firmware embedded in the DSP 4. The DSP 4 then provides the data output unit 7 with data 8, which has completed the digital processing, with appropriate timing. The data output unit 7 then properly outputs the data 8 to a circuit at the next stage as data 9. It should be noted that the clock signal 6 for driving the operation of the DSP 4 is obtained by multiplying the frequency of the system clock 11 using the frequency multiplier 10.

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

End of Result Set

Generate Collection Print

L5: Entry 7 of 7 File: USPT Dec 31, 1991

DOCUMENT-IDENTIFIER: US 5077686 A

**** See image for Certificate of Correction ****

TITLE: Clock generator for a computer system

Detailed Description Text (35):

Thus, what has been described is a circuit which provides a clock signal (or plurality of clock signals) at a multiple of the system clock frequency allowing for design of a computer system having processor synchronized with a system clock and allowing the processors to run at a clock speed which is some multiple of the system clock speed. Thus, a multiple processor computer system may have some of its processors upgraded to higher speed processors while retaining some of the original, lower speed, processors in the system and the higher speed processors are run in lock step with system clock and, thus, in lock step with the lower speed processors.

Previous Doc Next Doc Go to Doc#

L23: Entry 2 of 5 File: USPT Mar 18, 2003

DOCUMENT-IDENTIFIER: US 6535926 B1
TITLE: Time synchronization system for industrial control network using global reference pulses

Brief Summary Text (4):
The present invention relates to industrial controllers used for real-time control of industrial processes and in particular to a method of synchronizing clocks among multiple industrial controllers connected by a network, wherein the synchronizing method is applicable to a wide variety of different network protocols.

Brief Summary Text (6):
An industrial controller differs from a conventional computer in that the various components of the industrial controller may be separated by a considerable distance commensurate with the expanse of a large factory or manufacturing operation. Separated industrial controllers communicate via digital messages transmitted over one or more communication networks including well-known standards of EtherNet, DeviceNet, ControlNet, Fire Wire, Field Bus, SERCOS and ATM. Each of these networks employs different communication protocols. Inter-communication among industrial controllers using different standards is facilitated by the availability of application-specific integrated circuits (ASIC) providing for low-level formatting and queuing operations necessary to interface to the communication media

Detailed Description Text (5):
The bus 22 also connects to a network interface 27 being typically an applications specific integrated circuit (ASIC) providing the protocols necessary for communication between the controllers 12 on the networks 14. Such protocols may include the open standard protocols of EtherNet, ControlNet, Field Bus, Fire Wire, GPS, Sercos, ATM and other protocols well known in the art. A human machine interface (HMI) 28 may also be connected to the bus 22 to provide for local control by operators of the equipment 16.

Current US Cross Reference Classification (2):
713/400

Current US Cross Reference Classification (4):
713/500

Current US Cross Reference Classification (5):
713/503

Current US Cross Reference Classification (6):
713/600